Compiling Polychronous Programs into Conditional Partial Orders for ASIP Synthesis

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with
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Motivation

Current trends in hardware requirements

- ↑Performance, ↓Latency, ↓Power Consumption, ↓Form Factor
- ↑Programmability for enabling reuse of components
- ↑Flexibility to introduce late specification changes
Current trends in hardware requirements

- \( \uparrow \) Performance, \( \downarrow \) Latency, \( \downarrow \) Power Consumption, \( \downarrow \) Form Factor
- \( \uparrow \) Programmability for enabling reuse of components
- \( \uparrow \) Flexibility to introduce late specification changes

Application Specific Instruction-set Processors (ASIPs)

- Designed to exploit special characteristics of class of applications
- Reuse of components based on programmable modes of operation
- Custom instruction sets allow to maintain a level of flexibility
- Balance between ASICs and general purpose processors
Design methodologies for ASIPs should provide,

- Compact & efficient way to describe & store instruction sets
- Identify parallelism and express modes of operation
- A way to express available and required resources and map them
- Encoding of instruction sets for various optimization criteria
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**Conditional Partial Order Graphs (CPOGs)** offer these facilities!
Outline of the talk

1. Motivation
2. Introduction to CPOGs
3. Introduction to MRICDF
4. MRICDF Models to CPOGs
5. Analysis and ASIP Synthesis
6. Conclusion and Future
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Conditional Partial Order Graphs

- A compact semantic model to express and compose large partial order sets
- Yields itself very easy for transformations, refinements, optimizations and encodings
- Graphically they can be visualised as hierarchical, annotated, weighted, directed graphs
Formally, CPOG is represented as a quintuple $G = \langle V, E, X, \rho, \phi \rangle$

- $V$ is a set of *nodes* which corresponds to events/atomic actions in a system that is being modelled.
- $E \subseteq V \times V$ is a set of directed *edges* between the *nodes*. An edge from node $n$ to node $m$, indicates action $m$ depends on $n$.
- $X$ is a set of $n$ Boolean variables. Each Boolean variable could be assigned values $\{0, 1\}$ resulting in unique $2^n$ possible codes.
- $\rho$ is a *restriction function* defined on the set of Boolean variables in $X$ as $\rho \in \mathcal{F}(X)$, where $\mathcal{F}(X)$ is the set of all Boolean functions on the Boolean variables in $X$.
- Function $\phi : (V \cup E) \rightarrow \mathcal{F}(X)$. It assigns a Boolean condition $\phi(z)$ to every node and edge $z$ in the graph $G$. 
Example of CPOG

Figure: Graphical representation of CPOG
Example: Simple adder/subtractor application

- Does add or subtract based on select signal
- Table below shows micro-steps of instructions for example

<table>
<thead>
<tr>
<th>Adder (A = A + B; select)</th>
<th>Subtractor (A = A - B; select)</th>
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<tbody>
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</tr>
<tr>
<td>$l_2$: Load B</td>
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</tr>
<tr>
<td>$l_3$: Compute A + B</td>
<td>$l_5$: Compute A - B</td>
</tr>
<tr>
<td>$l_4$: Store A</td>
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Create 5 nodes: $l_1$, $l_2$, $l_3$, $l_4$, $l_5$

Create 6 edges:
- $l_1$ select $\rightarrow$ $l_3$
- $l_2$ select $\rightarrow$ $l_3$
- $l_3$ select $\rightarrow$ $l_4$
- $l_1$ select $\rightarrow$ $l_5$
- $l_2$ select $\rightarrow$ $l_5$
- $l_5$ select $\rightarrow$ $l_4$

Create Boolean variable set $X = \{ \text{select} \}$

Establish $\rho$ and $\phi$ functions
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- Representing this instructions as CPOG $H$
  - Create 5 nodes: $l_1, l_2, l_3, l_4, l_5$
  - Create 6 edges: 
    - $l_1 \xrightarrow{select} l_3, l_2 \xrightarrow{select} l_3, l_3 \xrightarrow{select} l_4,$
    - $l_1 \xrightarrow{select} l_5, l_2 \xrightarrow{select} l_5, l_5 \xrightarrow{select} l_4$
  - Create Boolean variable set $X = \{select\}$
  - Establish $\rho$ and $\phi$ functions
Encoding

- Atomic actions $I_1$ and $I_2$ can be executed concurrently or sequentially.
- Atomic action $I_2$ has to be executed before $I_3$.
- Partial order on the set of micro-steps/atomic actions.
- Assigning values from the set $\{0, 1\}$ to variables of $X$, to get unique Boolean vectors.
- Unique vectors can be used as opcodes for instructions.
CPOG representing execution of Simple adder/subtractor application

Figure: (A) Graphical representation of CPOG $H$, (B) $H|_{select}$, (C) $H|_{select}$
Composition of Instruction sets

- Instruction is a pair $I = (\phi, H|_{select})$, where $\phi$ is the opcode and $H|_{select}$ is the partial order.
- Instruction set $\mathcal{IS}$ is a set of instructions - $\mathcal{IS} = \{I_1, I_2, ..\}$, such that each $I_k$ has a different opcode $\phi$. 

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Composition of Instruction sets

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- Instruction set $\mathcal{IS}$ is a set of instructions - $\mathcal{IS} = \{I_1, I_2, \ldots\}$, such that each $I_k$ has a different opcode $\phi$.
- Composition of 2 instruction sets $\mathcal{IS}_i$ and $\mathcal{IS}_k$:
  - Is defined as $\mathcal{IS}_i \cup \mathcal{IS}_k$
  - Is defined only when no instruction in set $\mathcal{IS}_i$ has the same opcode as any instruction in $\mathcal{IS}_k$
  - Is not defined if there exists 2 instructions with the same opcodes.
- Composition of more than 2 instruction sets is done by performing pairwise composition in arbitrary order.
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- Complexity of composition: Linear with respect to the total number of instructions.
MRICDF - Multi-Rate Instantaneous Communication Data Flow

- A Visual Language (with a textual substitute) to express a computation over concurrent streams of data
- MRICDF model is hierarchical composition of actors
- Actors are connected using channels
- Signal flows via channels

Figure: A simple MRICDF model
Definitions

Definition (Event)

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**Definition (Clock of a signal)**

Instant set \( \sigma(x) \) is also known as clock of signal denoted by \( \hat{x} \).
### Definitions

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**Definition (Synchronous Signals)**

Signals \( x \) and \( y \) are called **synchronous signals** iff \( \hat{x} = \hat{y} \)
Definition (Data Dependence Relation)

- Multiple signals being read/written in an instant have a partial order - Dependency order

\[ x \xrightarrow{[c]} y, \text{ indicates that the signal } y \text{ is dependent on } x, \text{ when condition } c \text{ is true} \]

- Data dependencies are not static, they change based on predicates
### MRICDF Actors

- MRICDF consists of 4 primitive actors
- Numerous derived actors, Ex: Logical And, Multiplication, etc
- Every actor has a predefined set of Rate Constraints
- User can specify various synchronization requirements by adding additional clock constraints

<table>
<thead>
<tr>
<th>Actor definition</th>
<th>Clock Relations</th>
<th>Data Dependency Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function $r = a \times b$</td>
<td>$\sigma(a) = \sigma(b) = \sigma(r)$ &lt;br&gt;$\hat{a} = \hat{b} = \hat{r}$</td>
<td>$a \rightarrow r$ &lt;br&gt;$b \rightarrow r$</td>
</tr>
<tr>
<td>Buffer $y = x \text{n init } v_1...v_n$</td>
<td>$\sigma(y) = \sigma(x)$ &lt;br&gt;$\hat{y} = \hat{x}$</td>
<td>No dependency</td>
</tr>
<tr>
<td>Sampler $y = x \text{ when } z$</td>
<td>$\sigma(y) = \sigma(x) \cap \sigma(z = \text{true})$ &lt;br&gt;$\hat{y} = \hat{x} \wedge [\hat{z}]$</td>
<td>$x \xrightarrow{[z]} y$</td>
</tr>
<tr>
<td>Merge $r = a \text{ default } b$</td>
<td>$\sigma(r) = \sigma(a) \cup \sigma(b)$ &lt;br&gt;$\hat{r} = \hat{a} \vee \hat{b}$</td>
<td>$a \rightarrow r$ &lt;br&gt;$b \xrightarrow{\hat{b} - \hat{a}} r$</td>
</tr>
</tbody>
</table>
Determining relations between clocks and analysing is done in a step called - Clock Calculus

Aim of clock calculus: To determine which signals participate in which reaction

The signal that participates in each and every reaction - Master Trigger - multiple master triggers possible

Clock of Master Trigger signal is Master Clock

Clocks of signals that aren’t master triggers can be derived based on predicates of either master clock or clocks of other known signals

Hierarchically ordering these clocks gives us Hierarchial Clock Relation Graph (HCRG)

Rooted HCRG : Clock Tree
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CPOG for Function Actor

Operation: $y = f(x_1, x_2, .., x_n)$, Clock relation: $\hat{y} = \hat{x}_1 = \hat{x}_2 = .. = \hat{x}_n$

- $V = \{y, x_1, x_2, ..., x_n\}$
- $E = \{x_i \rightarrow y \mid x_i \in (x_1, x_2, ..., x_n)\}$
- $X = \{\{b_y\} \cup \{b_{x_i} \mid x_i \in (x_1, x_2, ..., x_n)\}\}$
  \[ b_y = b_{x_1} = b_{x_2} = ... = b_{x_n} \]

Function $\phi$

\[
\begin{align*}
\phi(y) &= b_y, \\
\phi(x_1) &= b_{x_1}, \\
&\vdots \\
\phi(x_n) &= b_{x_n}, \\
\phi(x_1 \rightarrow y) &= b_{x_1}, \\
\phi(x_2 \rightarrow y) &= b_{x_2}, \\
&\vdots \\
\phi(x_n \rightarrow y) &= b_{x_n}
\end{align*}
\]

Figure: CPOG for Function Actor
CPOG for Buffer Actor

Operation: \( y = x \) \( \text{init} \ c \)

Clock relation: \( \hat{y} = \hat{x} \)

- \( V = \{y, x\} \)
- \( E = \{\} \)
- \( X = \{b_y, b_x\} \)
- \( \rho = \{b_y = b_x\} \)
- Function \( \phi \)
  \[ \phi(y) = b_y \]
  \[ \phi(x) = b_x \]

\[ x : b_x \quad \bigcirc \quad \bigcirc y : b_y \]

Figure: CPOG for Buffer Actor

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CPOG for Sampler Actor

Operation: \( y = x \) when \( c \)

Clock relation: \( \hat{y} = \hat{x} \times [c] \)

- \( V = \{ y, x, c \} \)
- \( E = \{ x \rightarrow y, c \rightarrow y \} \)
- \( X = \{ b_y, b_x, b_c, b_{[c]}, b_{[\bar{c}]} \} \)

\[
\rho = \left\{ \begin{array}{l}
\{ b_y = b_x \land b_{[c]} \} \cup \\
\{ b_c = b_{[c]} \lor b_{[\bar{c}]} \} \cup \\
\{ b_{[c]} \land b_{[\bar{c}]} = false \}
\end{array} \right. 
\]

Function \( \phi \)

- \( \phi(y) = b_y \)
- \( \phi(x) = b_x \)
- \( \phi(c) = b_c \)

Figure: CPOG for Sampler Actor
CPOG for Merge Actor

Operation: \( y = x \text{ default } z \)
Clock relation: \( \hat{y} = \hat{x} + \hat{z} \)

- \( V = \{ y, x, z \} \)
- \( E = \{ x \rightarrow y, z \rightarrow y \} \)
- \( X = \{ b_y, b_x, b_z \} \)
- \( \rho = \{ b_y = b_x \lor b_z \} \)
- Function \( \phi \)
  - \( \phi(y) = b_y \)
  - \( \phi(x) = b_x \)
  - \( \phi(z) = b_z \)
  - \( \phi(x \rightarrow y) = b_x \)
  - \( \phi(z \rightarrow y) = b_z \land \bar{b}_x \)

Figure: CPOG for Merge Actor
Observations

Observation

For each primitive actor $A$, if $g_A$ represents the CPOG derived using the steps described above, then $g_A$ contains all the necessary information for control of scheduling the execution of $A$.

Observation

For primitive actors $A_1$ and $A_2$, if $g_{A_1}$ and $g_{A_2}$ represents the corresponding CPOGs then for composition $A_1 \mid A_2$, the corresponding CPOG is the $g_{A_1} \cup g_{A_2}$.
Deriving CPOG for Composite Actor

- Combination of primitive actors that are used to express modular and hierarchical behavior
- First we derive the CPOGs of composite actors and then compose (∪) it with the CPOG of the rest of the model
- Algorithm 1 lists the method used to derive a CPOG for a composite actor
Algorithm 1: Algorithm to derive CPOG for a Composite Actor

Input: Composite Actor CA, Model M
Output: CPOG $G = \langle V, E, X, \rho, \phi \rangle$ for CA
Initialize $G = \langle \{\}, \{\}, \{\}, \{\}, \{\} \rangle$;

Let $A_{NC} \& A_C$ be partition of actors in CA into sets of Primitive(Non-composite) and Composite actors resp. (present immediately under CA);
Let $I_{CA} = \{p_1, p_2, \ldots, p_n\}$ be the inports of CA;
Let $O_{CA} = \{p_1, p_2, \ldots, p_m\}$ be the outports of CA;

foreach composite actor $a \in A_C$ do
    //recursive call, $\cup$ represents composition of CPOGs
    $G \leftarrow G \cup \text{composite}_\text{cpog}(a, M)$;
end

foreach primitive actor $a \in A_{NC}$ do
    //\$U$ represents composition of CPOGs
    $G \leftarrow G \cup \text{primitive}_\text{cpog}(a)$;
end

foreach $p_i \in I_{CA} \cup O_{CA}$ do
    Let $c_{in}$ be the in-coming channel connected to $p_i$;
    Let $p_{ein}$ be source port of the channel $c_{in}$;
    
    foreach out-going channel $c_{out}$ from $p_i$ do
        Let $p_{eout}$ be destination port of channel $c_{out}$;
        Let $e_{new} = \text{createEdge}(p_{ein}, p_{eout})$;
        $E \leftarrow E \cup \{e_{new}\}$;
        $\phi(e_{new}) = \text{Constraints on } c_{in} \&\& \text{Constraints on } c_{out}$;
    end
end

return $G$;
Sample MRICDF model & its SIGNAL code

ADD, Comparator, GAIN & $\frac{1}{GAIN}$ are predefined function actors

```
function process = (?int i1, i2, sel; !int out;)
  | sig1 = GAIN(i1)
  | sig3 = 1/GAIN(i1)
  | sig2 = ADD(sig1, in2)
  | sig4 = ADD(sig2, in2)
  | sig5 = (sel >= 0)
  | sig6 = sig2 when sig5
  | sig7 = sig2 when not sig5
  | out = sig6 default sig7
)
where
  integer sig1,sig2,sig3,sig4,sig5,sig6,sig7;
end;
```
CPOG for the Example MRICDF model

Figure: CPOG for the MRICDF Model
Formal representation CPOG for the Example MRICDF model

<table>
<thead>
<tr>
<th>Quintuple Element</th>
<th>Set Elements</th>
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<tr>
<td>$V$</td>
<td>${in1, in2, sel, out, sig1, sig2, sig3, sig4, sig5, sig6, sig7}$</td>
</tr>
<tr>
<td>$E$</td>
<td>${in1 \rightarrow sig1, in1 \rightarrow sig3, in2 \rightarrow sig2, in2 \rightarrow sig4, sig3 \rightarrow sig4, sig1 \rightarrow sig2, sig2 \rightarrow sig6, sig4 \rightarrow sig7, sel \rightarrow sig5, sig5 \rightarrow sig6, sig5 \rightarrow sig7, sig6 \rightarrow out, sig7 \rightarrow out}$</td>
</tr>
<tr>
<td>$X$</td>
<td>${b_{x1}, b_{x2}, b_{x3}, b_{x4}, b_{x5}, b_{x6}, b_{x7}, b_{x8}, b_{[x8]}, b_{\overline{x8}}, b_{x9}, b_{x10}, b_{x11}}$</td>
</tr>
<tr>
<td>$\rho$</td>
<td>${b_{x1} = b_{x2} = b_{x3} = b_{x4} = b_{x5} = b_{x6} = m, b_{x7} = b_{x8} = n, b_{x8} = b_{[x8]} \lor b_{\overline{x8}}, false = b_{[x8]} \land b_{\overline{x8}}, b_{x9} = b_{x5} \land b_{[x8]}, b_{x10} = b_{x6} \land b_{[x8]}, b_{x11} = b_{x9} \lor b_{x10}}$</td>
</tr>
<tr>
<td>$\phi$</td>
<td>${\phi(in1) = b_{x1}, \phi(in2) = b_{x2}, \phi(sig1) = b_{x3}, \phi(sig2) = b_{x5}, \phi(sig3) = b_{x4}, \phi(sig4) = b_{x6}, \phi(sel) = b_{x7}, \phi(sig5) = b_{x8}, \phi(sig6) = b_{x9}, \phi(sig7) = b_{x10}, \phi(out) = b_{x11}, \phi(in1 \rightarrow sig1) = b_{x1}, \phi(in1 \rightarrow sig3) = b_{x1}, \phi(in2 \rightarrow sig2) = b_{x2}, \phi(in2 \rightarrow sig4) = b_{x2}, \phi(sig1 \rightarrow sig2) = b_{x3}, \phi(sig3 \rightarrow sig4) = b_{x4}, \phi(sig2 \rightarrow sig6) = b_{x5} \land b_{[x8]}, \phi(sig4 \rightarrow sig7) = b_{x6} \land b_{\overline{x8}}, \phi(sel \rightarrow sig5) = b_{x7}, \phi(sig5 \rightarrow sig6) = b_{x5} \land b_{[x8]}, \phi(sig5 \rightarrow sig7) = b_{x6} \land b_{[x8]}, \phi(sig6 \rightarrow out) = b_{x9}, \phi(sig7 \rightarrow out) = b_{x10} \land b_{\overline{x9}}}$</td>
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Initial CPOG needs to be simplified before transformations are applied

- Aim is to reduce the number of variables in set $X$
- Use the equivalence relations in set $\rho$
- Algorithm 2 lists the simplification step

**Algorithm 2: simplify($G$): Simplify CPOG**

**Input:** Un-simplified CPOG $G =$ $\langle V, E, X, \rho, \phi \rangle$

**Output:** Simplified CPOG $G =$ $\langle V, E, X, \rho, \phi \rangle$

Let $\mathcal{E} =$ $\{$Set of all Boolean equalities among single literals in $\rho$$\}$$;$
Let $\langle b_{x_1}, b_{x_2}, \ldots, b_{x_n} \rangle$ represent the vector $X$;

foreach $b_{xi} \in V$ do

    if $(b_{xi} = b_{xj}) \in \mathcal{E}$ then

        replace all occurrences of $b_{xj}$ in $\rho$ and $\phi$ and simplify with idempotence and other Boolean simplification laws to obtain new $\rho$, and new $\phi$.

        $X = X - \{b_{xj}\}$;

    end

end
Proposition

**Algorithm 2 converges and reduces the number of control states of the resulting system**

**Proof:** Convergence is based on number of equivalence classes of control variables in $X$, and its reduction in each step

- Number of control states can be reduced further by proving more Boolean equivalences using powerful solvers like SMT solver
- Another way to reduce control states is by eliminating equivalent behaviors
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- $X$ is simplified

Set of assignments for variables in $X$ that results in feasible behaviors: 1101, 1110
Propagate feasible behavior assignments onto CPOGs to get feasible CPOGs

- Nodes and edges with value 0 are eliminated
- Node is excluded, if all the incoming edges to a node are excluded
- Node is excluded, if all the outgoing edges of a node are excluded
- All edges originating from an excluded node are also excluded
- All edges terminating on an excluded node are also excluded
- All other nodes and edges are left as such

Algorithm 3 provides the set of feasible CPOGs
Algorithm 3: getFeasibleCPOGs($G, F$)

**Input:** Simplified CPOG $G = (V, E, X, \rho, \phi)$, Feasible behavior assignments for $X$ as $F = \{\langle f_1 \rangle, \ldots, \langle f_k \rangle\}$  
//Ex:  
\[ F = \{<1101>, <1110>\} \]

**Output:** Set of CPOGs $\mathcal{V} = \{G_1, G_2, \ldots, G_k\}$

Let $\mathcal{V} = \{\}$;

foreach feasible behavior $f_i \in F$ do

Let $G_i$ be an instance of $G$;

foreach node or edge $z \in G_i$ do

//Evaluate $\phi(z)$ based on $f_i$ value

if $\phi(z) | f_i == 0$ then

$G_i = G_i - \{z\}$; //Remove $z$ from CPOG

//Remove unused edges

if $z$ is node then

Remove all incoming edges to $z$ and Remove all outgoing edges from $z$;

end

end

end

//Remove isolated nodes

foreach remaining node $z \in G_i$ do

Let $I_z$ be the set of incoming edges to $z$ and let $O_z$ be the set of outgoing edges from $z$;

if $I_z == \{\}$ or $O_z == \{\}$ then

$G_i = G_i - \{z\}$; //Remove node $z$ from CPOG

end

end

$\mathcal{V} \leftarrow \mathcal{V} \cup G_i$; //Add $G_i$ to set $\mathcal{V}$

end

return $\mathcal{V}$;
Feasible CPOGs with Boolean vector 1101 and 1110

Sandeep K. Shukla, FERMAT Lab, Virginia Tech.
CPOG has 11 nodes

Assuming each node requires a computation resource, we need 11 computation resources
Feasible CPOG with $X = 1101$ has 8 nodes
We only require 8 computation resources
Feasible CPOG with $X = 1110$ has 8 nodes

We only require 8 computation resources

The assignments $X = 1101, 1110$ can be used as opcodes and one can measure latency, power consumption etc in each mode.
Propagate feasible behaviors assignment values to the CPOG

- CPOG remains still *connected* and *rooted*
- No causal loops

Then the CPOG is sequentially implementable

Algorithm 4 checks the implementability

**Algorithm 4: isImplementable(G)**

<table>
<thead>
<tr>
<th>Input:</th>
<th>Simplified CPOG ( G = \langle V, E, X, \rho, \phi \rangle ), Feasible behavior assignments for ( X ) as ( F = { \langle f_1 \rangle, ..., \langle f_k \rangle } )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output:</td>
<td>True if implementable, else false</td>
</tr>
</tbody>
</table>

Let \( \mathcal{V} = \text{getFeasibleCPOGs}(G, F) \);

foreach CPOG \( G_i \in \mathcal{V} \) do

- if \( G_i \) has causal loops OR \( G_i \) is not weakly connected then
  - return false;

end

return True;
Outline of the talk

1. Motivation
2. Introduction to CPOGs
3. Introduction to MRICDF
4. MRICDF Models to CPOGs
5. Analysis and ASIP Synthesis
6. Conclusion and Future
Conclusion

- Proposed a new compilation scheme for SIGNAL/MRICDF polychronous specifications based on CPOGs
- Provided algorithms to derive CPOGs from SIGNAL/MRICDF specifications

Future Work

- Explore the aspect of sequential and concurrent implementability by applying transformations on the CPOGs
- Formal proofs
Further Reading for CPOGs and ASIPs

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*HDL Coder: Generate Verilog and VHDL code for FPGA and ASIC Designs*
Further Reading for MRICDF and Polychrony

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  *An alternative polychronous model and synthesis methodology for model-driven embedded software – ASP-DAC 2010*

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  *A novel technique for correct-by-construction concurrent code synthesis from polychronous specifications – ACSD 2013*

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  *Faster Software Synthesis Using Actor Elimination Techniques for Polychronous Formalism – ACSD 2010*

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Any Questions??

Thank You!!